This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device having a wiring pattern that is formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a separation from the contact section shorter than a ~~specified~~ predetermined separation; and

a second wiring having a connection region connected to the contact section,

wherein the second wiring has an extension section, which extends from a side of the connection region ~~extending~~ in a non-wiring region ~~in the connection region connected to the contact section~~, and

the extension section extends from at least one section of the connection region other than sides of the ~~connections~~ connection region facing the first wiring, wherein the extension section does not extend from the side of the connection region facing the first wiring.

2. (Currently Amended) The semiconductor device according to claim 1, wherein [the separation is shorter than a specified separation and] there is a minimum separation between wirings in the wiring pattern.

3. (Previously Amended) The semiconductor device according to claim 1, wherein the connection region is square in its plan configuration having dimensions that are greater than or equal to dimensions of the contact section.

4. (Previously Amended) The semiconductor device according to claim 1, wherein the extension section has an identical width as a width of the wiring.

5. (Previously Amended) The semiconductor device according to claim 1, wherein the extension section has an extension length identical with the width of the wiring.

6. (Previously Amended) The semiconductor device according to claim 1, wherein the extension section is square in its plan configuration.

7. (Currently Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a [minimum] predetermined inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and extending in parallel with the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non- wiring region in the connection region, and

the extension section does not extend from a ~~is disposed on~~ sides of the connection region ~~other than sides thereof~~ facing the first wiring.

8. (Currently Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a [minimum] predetermined inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section does not extend from a ~~is disposed on~~ sides of the connection region ~~other than sides thereof~~ facing the first wiring.

9. (Currently Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a [minimum] predetermined inter-wiring separation with respect to the contact section; and

a second wiring having a connection region to be connected to the contact section and having a section extending in parallel with the first wiring and a section extending in a direction perpendicular to the first wiring,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section does not extend from a ~~is disposed on~~ sides of the connection region ~~other than sides thereof~~ facing the first wiring.

10. (Currently Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a first wiring formed over the interlayer dielectric layer and disposed with a [minimum] predetermined inter-wiring separation with respect to the contact section; and

a second wiring having only a connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region; and

the extension section does not extend from a ~~is disposed on~~ sides of the connection region ~~other than sides thereof~~ facing the first wiring.

11. (Currently Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer;

a plurality of first wirings formed over the interlayer dielectric layer and disposed with a [minimum] predetermined inter-wiring separation with respect to the contact section; and

a second wiring having at least one connection region to be connected to the contact section,

wherein the connection region of the second wiring has a generally square plan configuration,

the second wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section does not extend from a ~~is disposed on~~ sides of the connection region ~~other than sides thereof~~ facing the plurality of first wirings.

12. (Currently Amended) A semiconductor device having a wiring pattern formed by etching a conductive layer using a resist pattern as a mask, the semiconductor device comprising:

a contact section formed in an interlayer dielectric layer; and

a wiring having a connection region to be connected to the contact section,

wherein the connection region of the wiring has a generally square plan configuration, and

the wiring has an extension section extending in a non-wiring region in the connection region, and

the extension section does not extend from a side of the connection region facing the plurality of first wirings.

13. (Previously Amended) The semiconductor device according to claim 12, wherein the wiring is line-like in shape and has extension sections on three sides of the connection region.

14. (Cancelled) The semiconductor device according to claim 12, wherein the wiring is formed from the connection region and has extension sections on four sides of the connection region.

15.-20. (Cancelled)

21. (Previously Added) The semiconductor device according to claim 7, wherein the separation is shorter than a specified separation and there is a minimum separation between wirings in the wiring pattern.

22. (Previously Added) The semiconductor device according to claim 7, wherein the connection region is square in its plan configuration having dimensions that are greater than or equal to dimensions of the contact section.

23. (Previously Added) The semiconductor device according to claim 7, wherein the extension section has an identical width as a width of the wiring.

24. (Previously Added) The semiconductor device according to claim 7, wherein the extension section has an extension length identical with the width of the wiring.

25. (Previously Added) The semiconductor device according to claim 8, wherein the separation is shorter than a specified separation and there is a minimum separation between wirings in the wiring pattern.

26. (Previously Added) The semiconductor device according to claim 8, wherein the connection region is square in its plan configuration having dimensions that are greater than or equal to dimensions of the contact section.

Please add new claims 27-33 as follows:

27. (New) The semiconductor device according to claim 1, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section extends from at least the first side of the connection region and does not extend from the second side.

28. (New) The semiconductor device according to claim 7, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section is disposed on at least the first side of the connection region and is not disposed on the second side.

29. (New) The semiconductor device according to claim 8, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section is disposed on at least the first side of the connection region and is not disposed on the second side.

30. (New) The semiconductor device according to claim 9, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section is disposed on at least the first side of the connection region and is not disposed on the second side.

31. (New) The semiconductor device according to claim 10, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section is disposed on at least the first side of the connection region and is not disposed on the second side.

32. (New) The semiconductor device according to claim 11, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section is disposed on at least the first side of the connection region and is not disposed on the second side.

33. (New) The semiconductor device according to claim 12, wherein the connection region has a first side and a second side that faces the first wiring, and wherein the extension section is disposed on at least the first side of the connection region and is not disposed on the second side.